IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A system for reducing power consumption in digital circuits using charge redistribution, comprising:

[[-]] a plurality of signal lines;

[[-]] an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to each said signal line that isolates said line from its source by placing said line in a high impedance state and that connects [[it]] said line to the intermediate floating virtual source/sink during an idle period prior to a change of state.

2. (Original) The system as claimed in claim 1 wherein the intermediate floating virtual source/sink comprises a charge storage element.

3. (Currently Amended) The system as claimed in claim 1 wherein the charge redistribution circuit ~~comprising the~~ comprises a transition detector connected to one of the signal lines and having two outputs, ~~one of which is~~ a first of the outputs connected to [[the]] an input of a tri-state driver circuit, ~~and the other~~ a second of the outputs for simultaneously ~~disable~~ (i) enabling the tri-state driver circuit to place the signal line in the high impedance state [[,]] and ~~enables the~~ (ii) enabling a control switch to connect [[its]] an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on [[a]] the signal line.

4. (Currently Amended) The system as claimed in claim 2 wherein the charge storage element ~~is~~ comprises a capacitor or a set of capacitors.

5. (Currently Amended) The system as claimed in claim 3 wherein the transition detector comprises [[ing]] a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detector and to [[the]] a first input of a 2-input exclusive-OR or exclusive-NOR gate while [[the]] a second input of the ~~exclusive-OR/ exclusive-NOR~~ gate is directly connected to the signal line and its output is connected to the second output of the [[T]] transition [[D]] detector.

6. (Currently Amended) The system as claimed in claim 4 wherein the capacitor comprises [[ing]] a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

7. (Currently Amended) An integrated circuit for reducing power consumption in digital circuits using charge redistribution, comprising:

a plurality of signal lines;

an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to each said signal line that isolates said line from its source by placing said line in a high impedance state and that connects [[it]] said line to the intermediate floating virtual source/sink during an idle period prior to a change of state.

8. (Original) An integrated circuit as claimed in claim 7 wherein the intermediate floating virtual source/sink comprises a charge storage element.

9. (Currently Amended) An integrated circuit as claimed in claim 7 wherein the charge redistribution circuit ~~comprising the~~ comprises a transition detector connected to one of the signal lines and having two outputs, ~~one of which is~~ a first of the outputs connected to [[the]] an input of a tri-state driver circuit, ~~and the other~~ a second of the outputs for simultaneously ~~disable~~ (i) enabling the tri-state driver circuit to place the signal line in the high impedance state [[,]] and ~~enables the~~ (ii) enabling a control switch to connect [[its]] an output of the tri-state driver circuit to the floating virtual source/sink whenever a transition is detected on [[a]] the signal line.

10. (Currently Amended) An integrated circuit as claimed in claim 8 wherein the charge storage element [[is]] comprises a capacitor or a set of capacitors.

11. (Currently Amended) An integrated circuit as claimed in claim 9 wherein the transition detector comprises [[ing]] a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detector [[s]] and to [[the]] a first input of a 2-input exclusive-OR or exclusive-NOR gate while [[the]] a second input of the ~~exclusive-OR/ exclusive-NOR fate~~ gate is directly connected to the signal line [[,]] and its output is connected to the second output of the [[T]] transition [[D]] detector.

12. (Original) An integrated circuit as claimed in claim 10 wherein the capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

13. (Currently Amended) A method for reducing power consumption in digital circuits using charge redistribution, comprising the steps of:

providing a plurality of signal lines;

providing an intermediate floating virtual source/sink, and

isolating each signal line from its source circuit by placing the signal line in a high impedance state and connecting [[it]] the signal line to the intermediate floating virtual source/sink during an idle period prior to a change of state.

14. (Currently Amended) The method as claimed in claim 13 wherein the step of providing an intermediate floating virtual source/sink comprises [[ing]] supplying a charge storage element.

15. (Original) The method as claimed in claim 13 wherein the change of state is identified by detecting a transition on the signal line.

16. (Original) The method as claimed in claim 14 wherein the charge storage element is supplied by connecting a capacitor or a set of capacitors.

17. (Currently Amended) The method as claimed in claim 15 wherein the transition is detected by exclusive-NORing or exclusive-ORing [[the]] a signal on the signal line with a delayed version of the signal.

18. (Currently Amended) The method as claimed in claim 15 wherein the signal line is connected to the intermediate floating virtual source/sink whenever [[a]] the transition is detected.

19. (Original) The method as claimed in claim 16 wherein the capacitor is provided by a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

20. (New) The method as claimed in claim 13, wherein isolating one of the signal lines from its source circuit and connecting the signal line to the intermediate floating virtual source/sink comprise:

enabling a tri-state driver circuit to place the signal line in the high impedance state; and

simultaneously enabling a control switch to connect an output of the tri-state driver circuit to the floating virtual source/sink.